AMENDMENTS TO THE SPECIFICATION

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please replace the paragraph starting on page 3, line 5 with the following paragraph:

FIG. 1 is a block diagram of a combined video and graphics processing system; ~~and~~

FIG. 2 is a block diagram of a BME of FIG. 1; and

FIG. 3 is a detailed block diagram of a composite circuit of FIG. 2.

Please add the following paragraphs starting after page 8, line 21:

Referring to FIG. 3, a detailed block diagram of the composite circuit 104 is shown. The circuit 104 generally comprises a circuit 140, a circuit 142, a circuit 144 and a circuit 146. The circuit 140 may be implemented as a logical operations circuit (block). The circuit 142 may be implemented as an alpha operations circuit (block). The circuit 144 may be implemented as an interleave operations circuit (block). The circuit 146 may be implemented as a multiplexer.

The composite circuit 104 may have an input 134 that may receive a signal (e.g., COMPTYPE). The signal COMPTYPE may be externally generated and written to a BMME control register by a CPU (both of which are not shown). The signal COMPTYPE may control the type of data combination operation carried out by the composite block 104. The various signals of the present invention may be implemented as multi-bit or single bit signals or busses.

The circuit 140 may have an input 150a that may receive the signal COMPTYPE, an input 152a that may receive the signal FRONT', an input 154a that may receive the signal BACK and an input 156a that may receive the signals MASK and/or ALPHA. Similarly, the circuits 142 and 144 may have, respectively, inputs 150b and 150c that may receive the signal COMPTYPE, inputs 152b and 152c that may receive the signal FRONT', inputs 154b and 154c that may receive the signal BACK and inputs 156b and 156c that may receive the signals MASK and/or ALPHA.

The circuit 140 may have an output 160 connected to an input 162 of the multiplexer 146. The circuit 142 may have an output 164 connected to an input 166 of the multiplexer 146. The circuit 144 may have an output 168 connected to an input 170 of the multiplexer 146. The multiplexer 146 may have an input 172 that may receive the signal COMPTYPE. The multiplexer 146 may present a signal received from the circuit 140, the circuit 142 or the

circuit 144 as the signal RESULT in response to the signal COMPTYPE.

The logical operations block 140 of the composite block 104 may implement logical bitwise operations such as:

RESULT = FRONT' XOR BACK

RESULT = (MASK AND FRONT') OR ((NOT MASK) AND BACK).

The alpha operations block 142 of the composite circuit 104 may perform alpha-blending equations such as:

RESULT = (ALPHA * FRONT') + ((1-ALPHA) * BACK)).

The interleave operations block 144 of the composite circuit 104 generally comprises multiplexers and bit shifters (not shown). The interleave operations block 144 may perform (but is not limited to) the following operations:

(i) take data from the signal FRONT' and pass the data unchanged to the signal RESULT, (the data may be chroma (U,V) pairs, or YUV, RGB, αYUV or αRGB pixels);

(ii) take chroma-only (U,V) data from the signal FRONT' and Y data from the signal BACK and combine the data to make up 24-bpp YUV values in the signal RESULT; and/or

(iii) take chroma-only (U,V) data from the signal FRONT', Y data from the signal BACK and alpha data from the signal ALPHA and combine the data to make up 32-bpp αYUV values in the signal RESULT.

Example operations of the interleave operations block 144 are shown in the following TABLES 1a and 1b.

TABLE 1a

Conversion	Front'				Back			
	31:24	23:16	15:8	7:0	31:24	23:16	15:8	7:0
4:2:0 to 4:4:4	U	V	U	V	-	-	-	-
4:2:2 to 4:4:4	U	V	U	V	-	-	-	-
4:4:4 to YUV	-	-	U	V	-	-	-	Y
4:4:4 to RGB	-	R	G	B	-	-	-	-
4:4:4 + alpha to αYUV	-	-	U	V	-	-	-	Y
αYUV to αRGB	A	R	G	B	-	-	-	-

TABLE 1b

Conversion	Mask/Alpha				Result			
	31:24	23:16	15:8	7:0	31:24	23:16	15:8	7:0
4:2:0 to 4:4:4	-	-	-	-	U	V	U	V
4:2:2 to 4:4:4	-	-	-	-	U	V	U	V
4:4:4 to YUV	-	-	-	-	-	Y	U	V
4:4:4 to RGB	-	-	-	-	-	R	G	B
4:4:4 + alpha to αYUV	-	-	-	A	A	Y	U	V
αYUV to αRGB	-	-	-	-	A	R	G	B

The entries in the TABLE 1a and the TABLE 1b may relate to the conversion operations of the interleave circuit 144 of the composite circuit 104. Input and output signals (e.g., the signal FRONT', the signal BACK, the signal MASK and/or ALPHA and the signal RESULT) may be 32-bits wide. Any color or alpha component

signal (e.g., RGB or alpha) may be 8-bits wide. However, other appropriate bit widths may be implemented to meet the criteria of a particular implementation. Additionally, some input bits may not be used in one or more conversion operations. Such unused bits may be omitted when applicable.